Figures from

Visualizing Parallel Logic Program Execution for Performance Tuning

Anthony J. Kusalik
Computer Science Dept.
University of Saskatchewan
Saskatoon, Saskatchewan
S7N 5A9 Canada
kusalik@cs.usask.ca

Steven D. Prestwich
ECRC GmbH
Arabellastr. 17
München 81925
Germany
steven@ecrc.de

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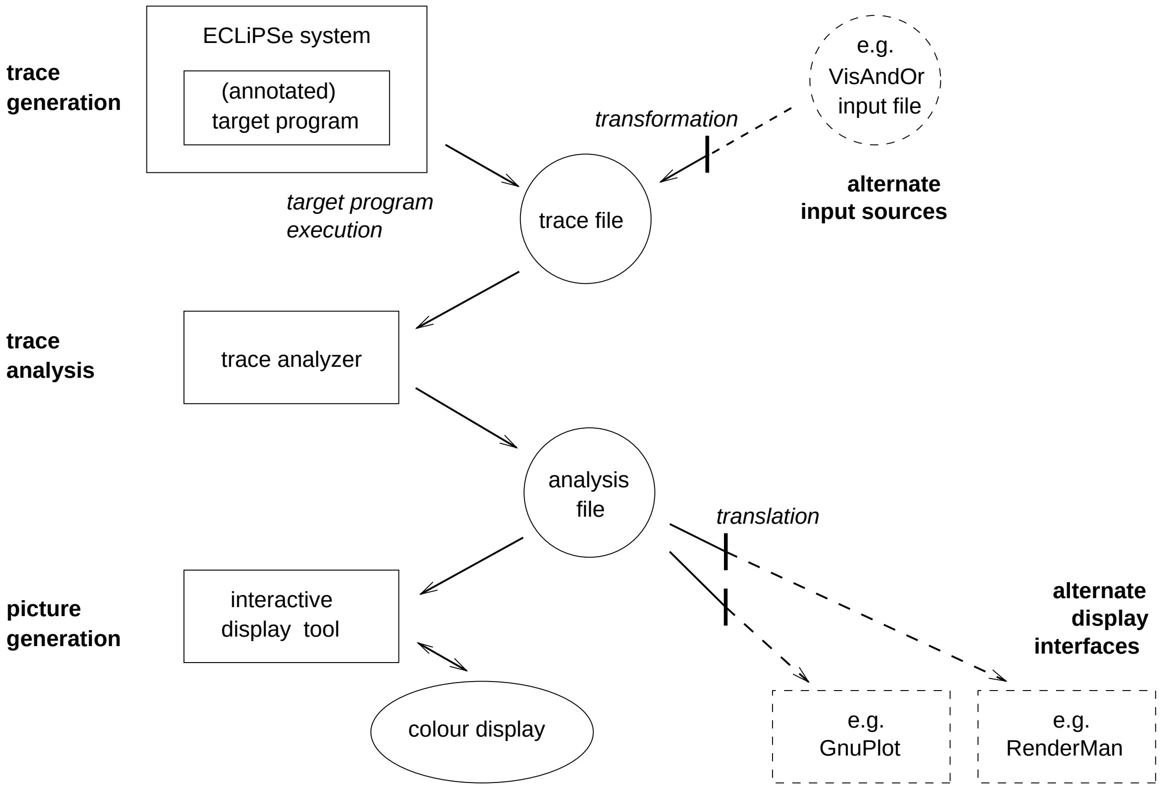

Figure 1: *Overview of the ParSee phases*

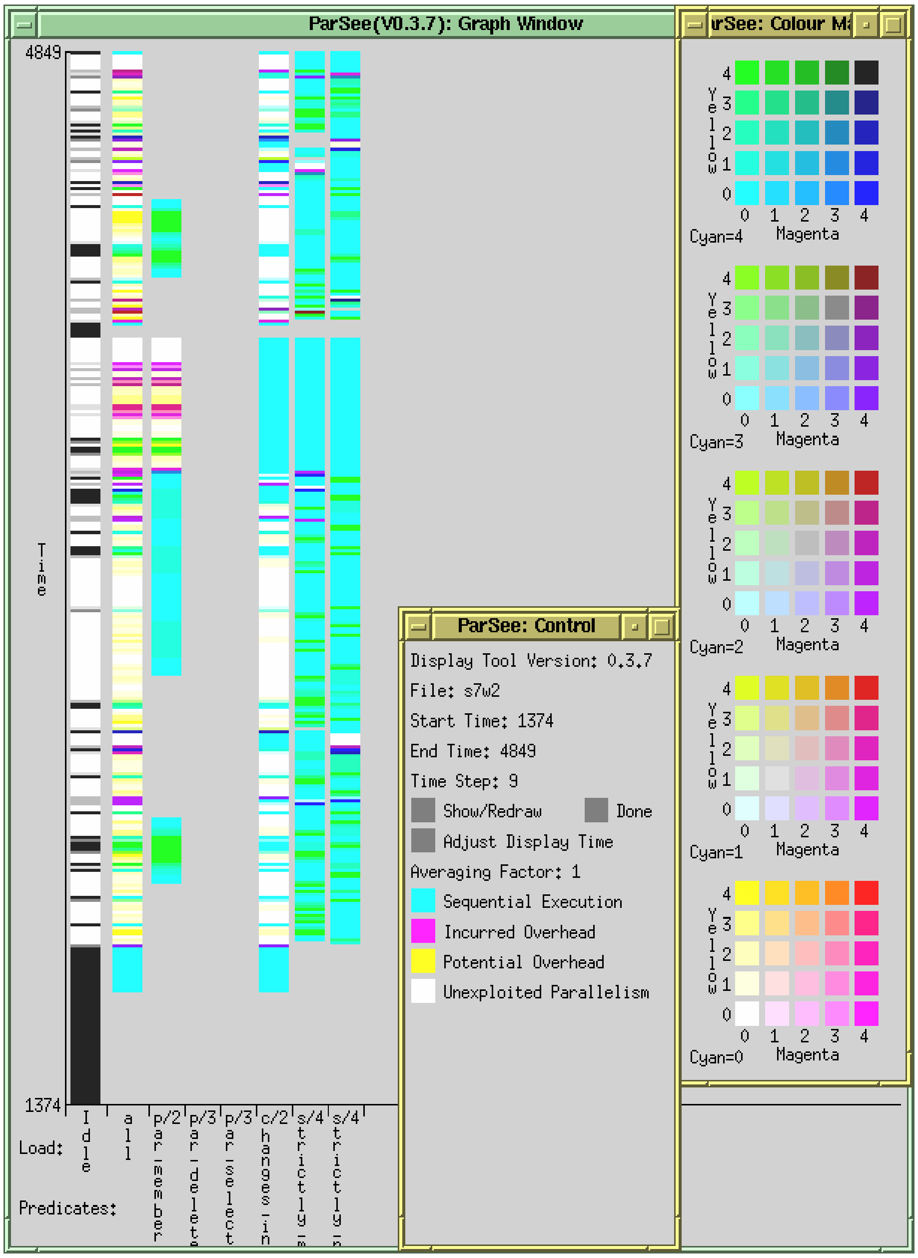

Figure 2: *Standard ParSee display interface*

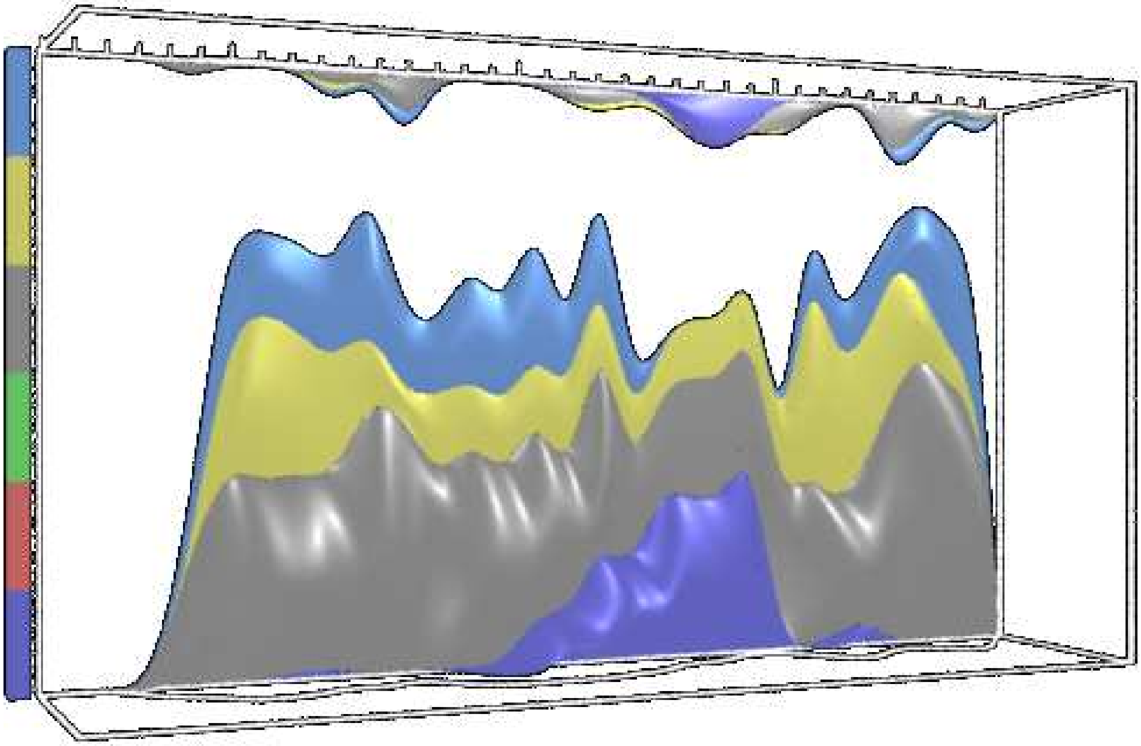

Figure 3: *Alternative ParSee display interface*

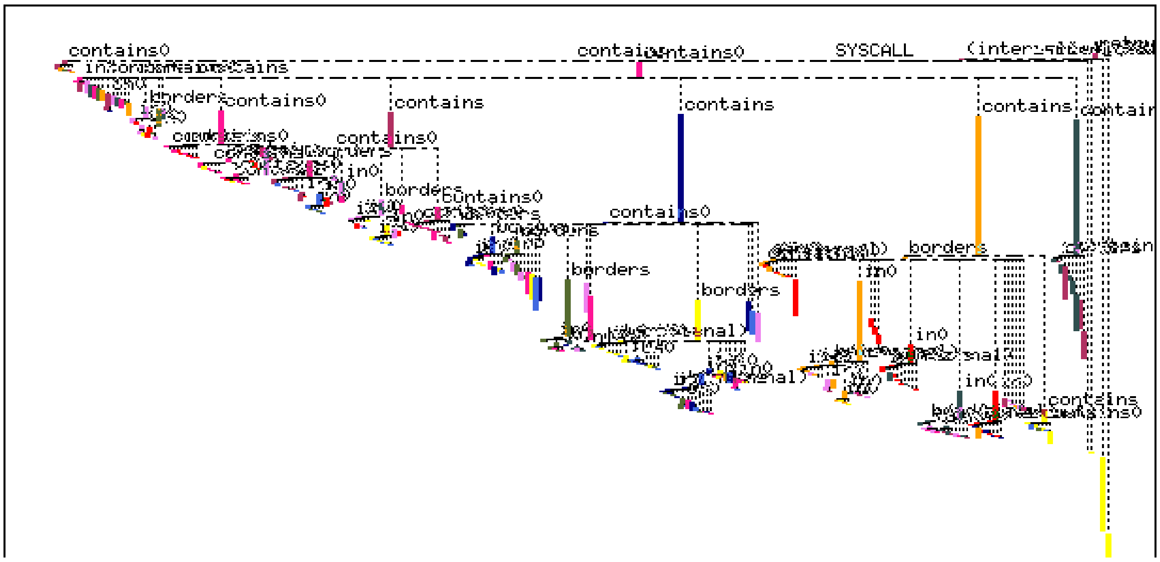

Figure 4: *Portion of a VisAndOr display of an Aurora computation*

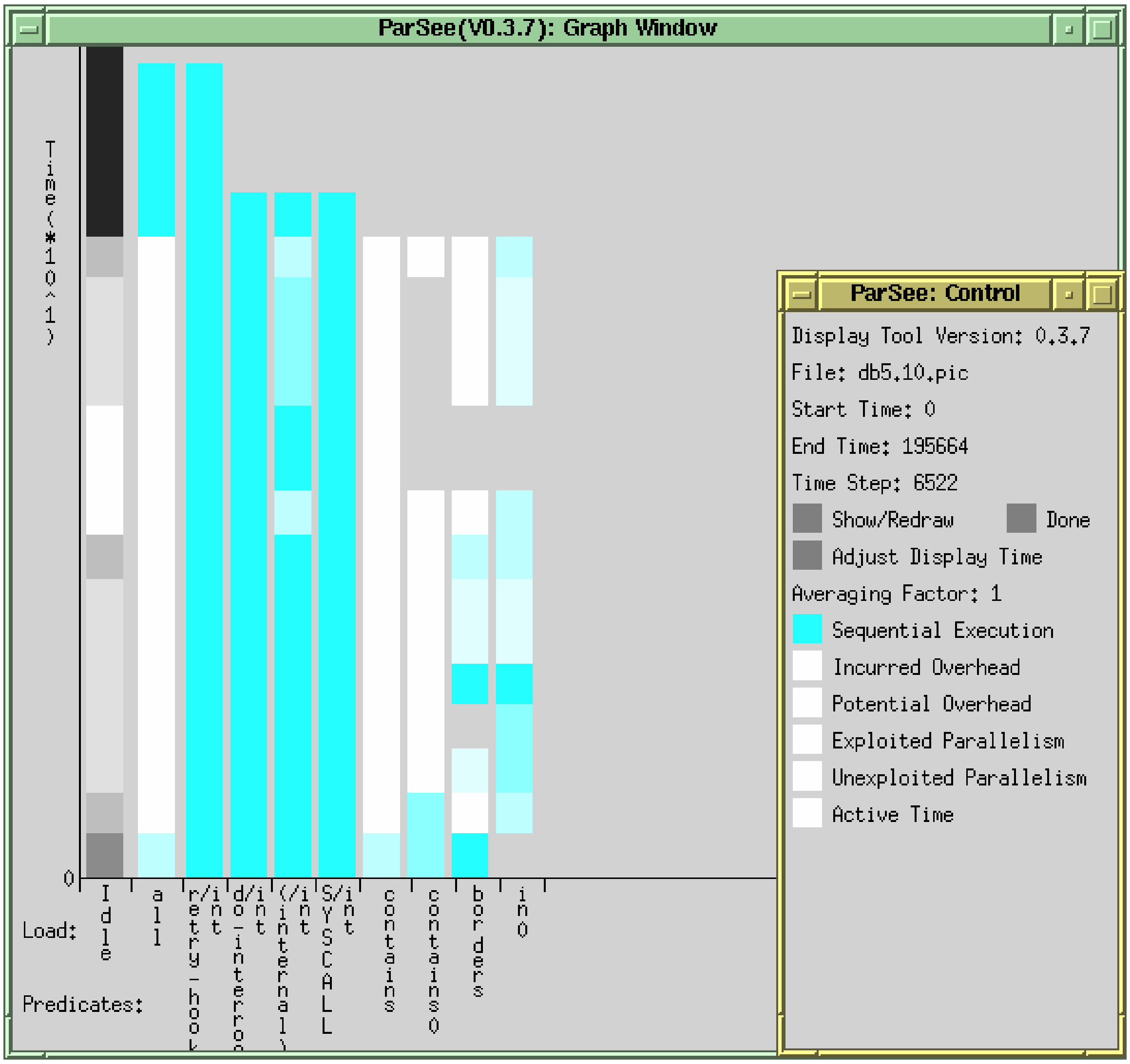

Figure 5: *ParSee display of Aurora computation*