Amdahl's Law in the Multicore Era

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November 26, 2009

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Reference:

- Mark D. Hill and Michael R. Marty, Amdahl's Law in the Multicore Era, *IEEE Computer*, 41(7), pp.33-38, July 2008, doi:10.1109/MC.2008.209

Outline

1. Introduction
   - Amdahl's Law Background
2. Three Types of Chip Designs and Speedup Equations
3. Simulation Results and Implications
   - Simulation Results
   - Implications

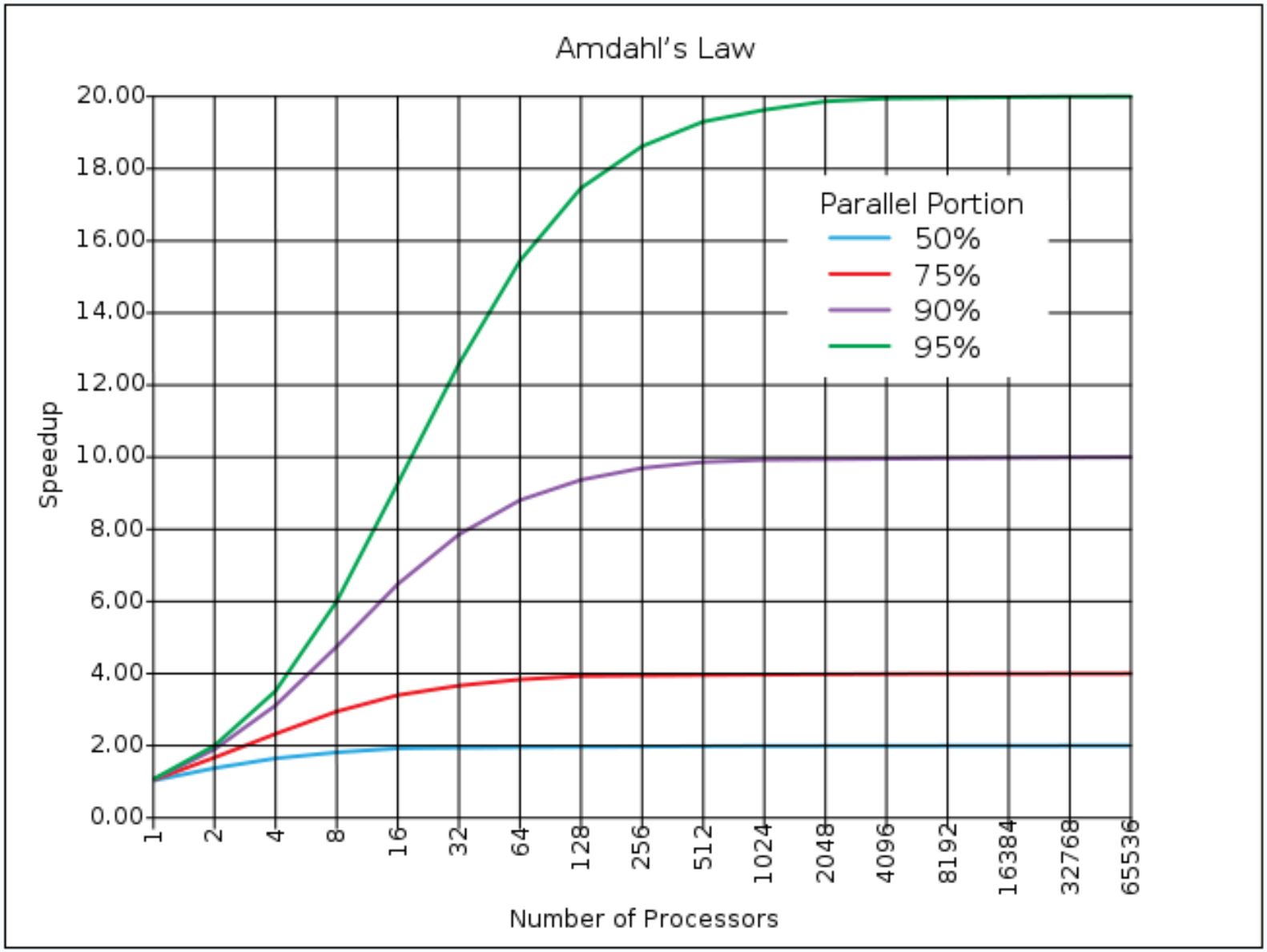
Amdahl's Law Background

- Is used to find the maximum expected improvement to an overall computer system.
- Is a model for the relationship between the expected speedup of parallelized implementations of an algorithm relative to the serial algorithm.

$$Speedup_{parallel}(f, n) = \frac{1}{(1 - f) + \frac{f}{n}} \quad (1)$$

- f: Fraction of computation that can be done in parallel. $f \in [0, 1]$
- n: Number of processors.

Amdahl's Law Background



Three Types of Chip Designs and Speedup Equations

- Symmetric Multicore Chips

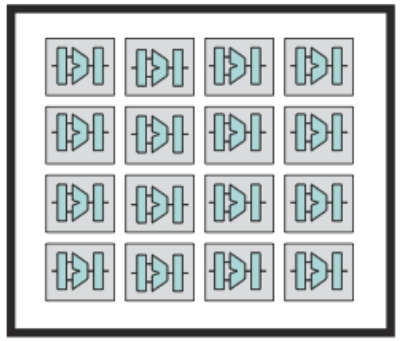


Figure: Sixteen 1-BCE cores

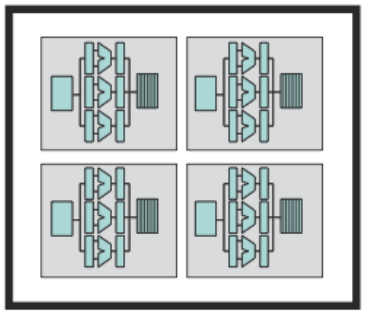
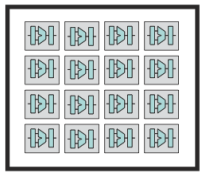


Figure: Four 4-BCE cores

Three Types of Chip Designs and Speedup Equations

Speedup Equation for Symmetric Multicore Chips:



$$Speedup_{symmetric}(f, n, r) = \frac{1}{\frac{1-f}{perf(r)} + \frac{f}{perf(r)*\frac{n}{r}}} \quad (2)$$

- n: total chip resources in Base Core Equivalents (BCEs)
- r: the BCE resources devoted to increase the performance of each core
- perf(r): the performance of the chip using one core to execute sequentially
- perf(r)*n/r: the performance of the chip using all n/r cores to execute in parallel

Three Types of Chip Designs and Speedup Equations

- Asymmetric Multicore Chips

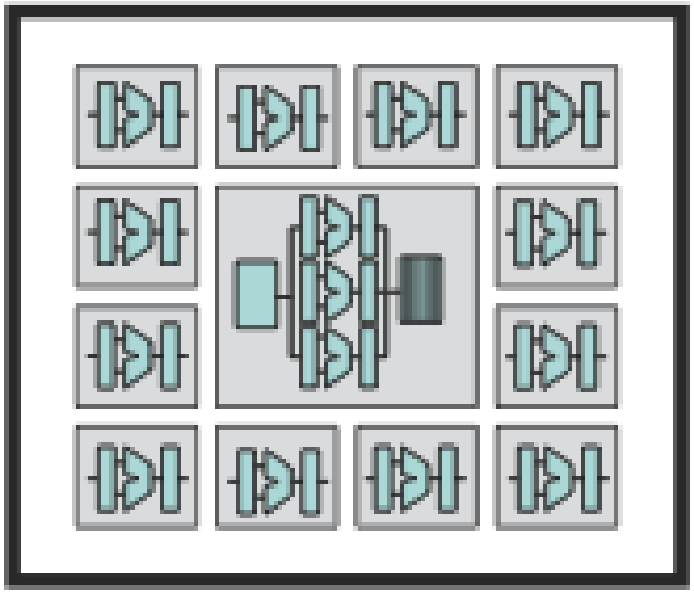
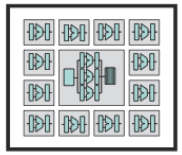


Figure: Asymmetric

1+n-r cores: Single r-BCE core and n-r 1-BCE cores

Three Types of Chip Designs and Speedup Equations

Speedup Equation for Asymmetric Multicore Chips:



$$Speedup_{asymmetric}(f, n, r) = \frac{1}{\frac{1-f}{perf(r)} + \frac{f}{perf(r)+n-r}} \quad (3)$$

- perf(r)+n-r: perf(r) from the large core and performance 1 from each of the n-r base cores

Three Types of Chip Designs and Speedup Equations

- Dynamic Multicore Chips

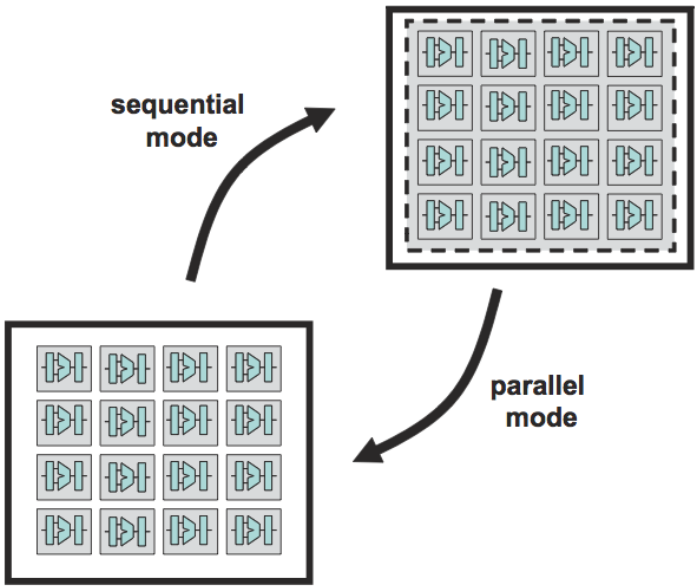
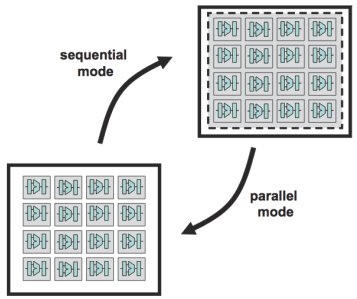


Figure: Dynamic

Three Types of Chip Designs and Speedup Equations

Speedup Equation for Dynamic Multicore Chips:



$$Speedup_{dynamic}(f, n, r) = \frac{1}{\frac{1-f}{perf(r)} + \frac{f}{n}} \quad (4)$$

A dynamic multicore gets performance n using all base cores in parallel

Simulation for Symmetric Chips

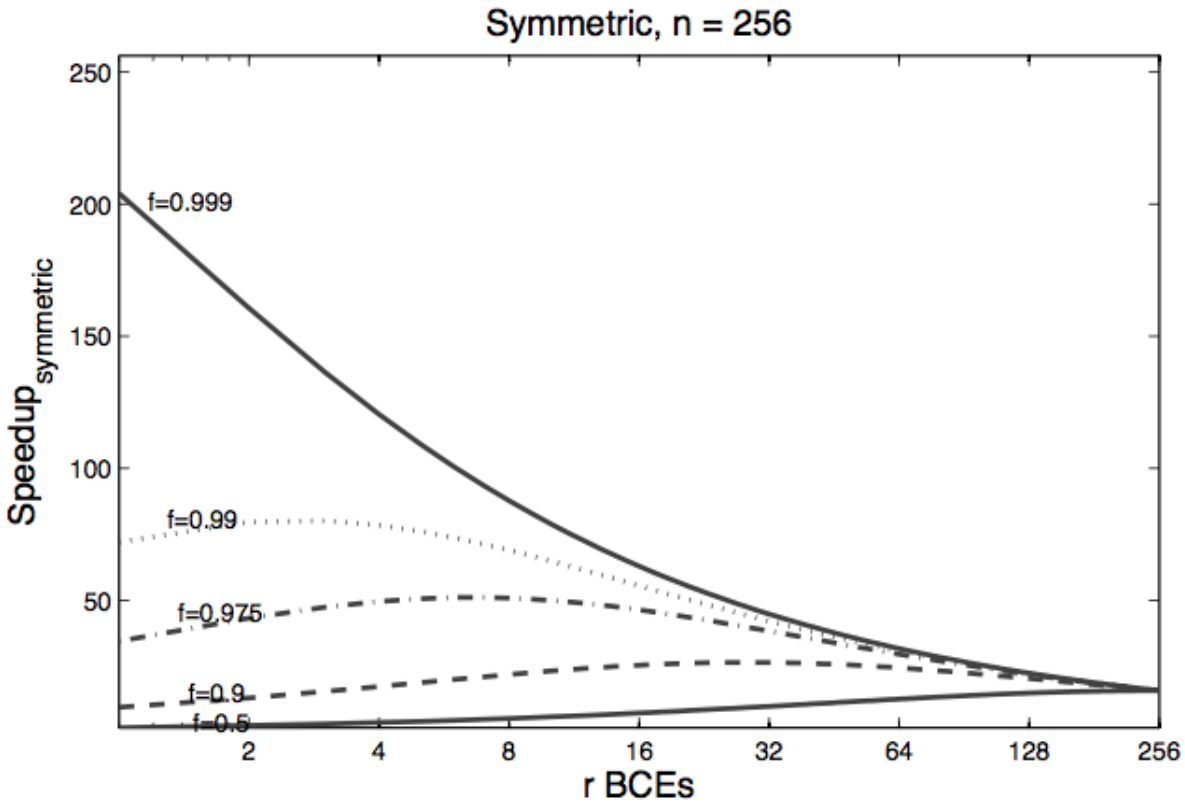


Figure: Speedup for symmetric chip design

$$f = 0.975 \ \textit{Best Speedup}_{\textit{symmetric}} = 51.2$$

Simulation for Asymmetric Chips

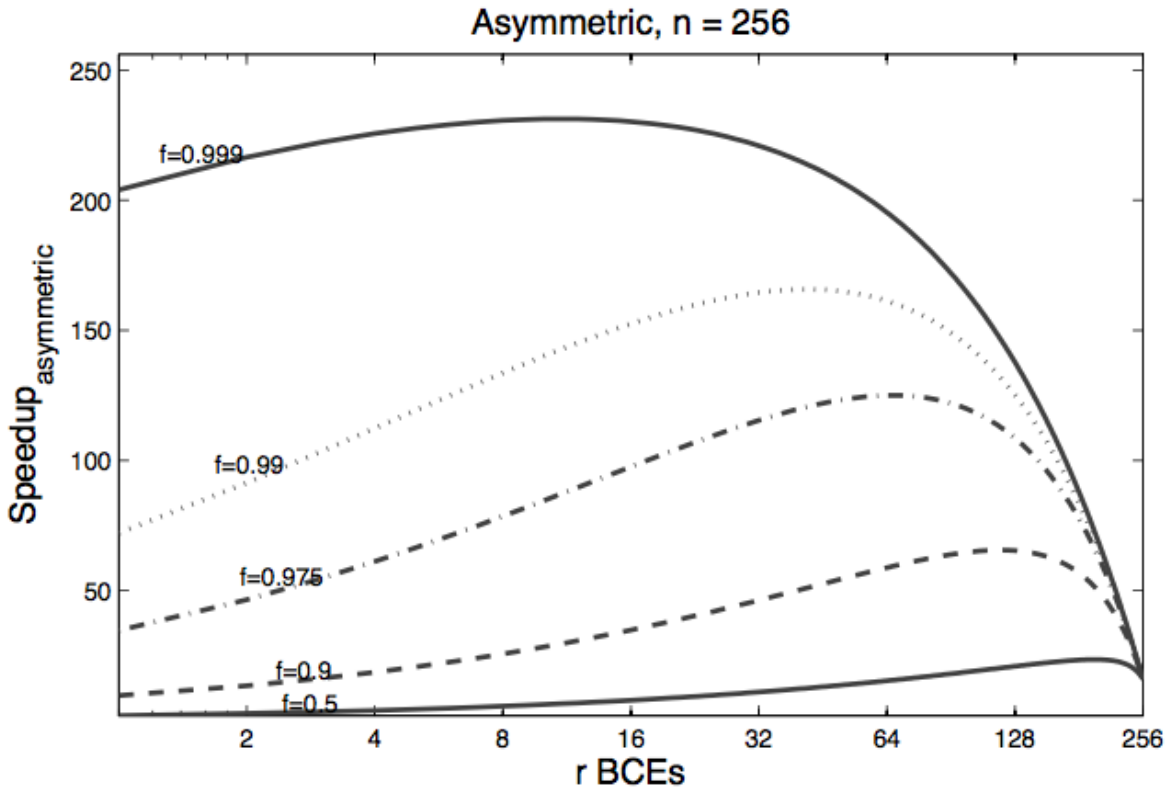


Figure: Speedup for asymmetric chip design

$$f = 0.975 \ \textit{Best} \ \textit{Speedup}_{\textit{asymmetric}} = 125.0$$

Simulation for Dynamic Chips

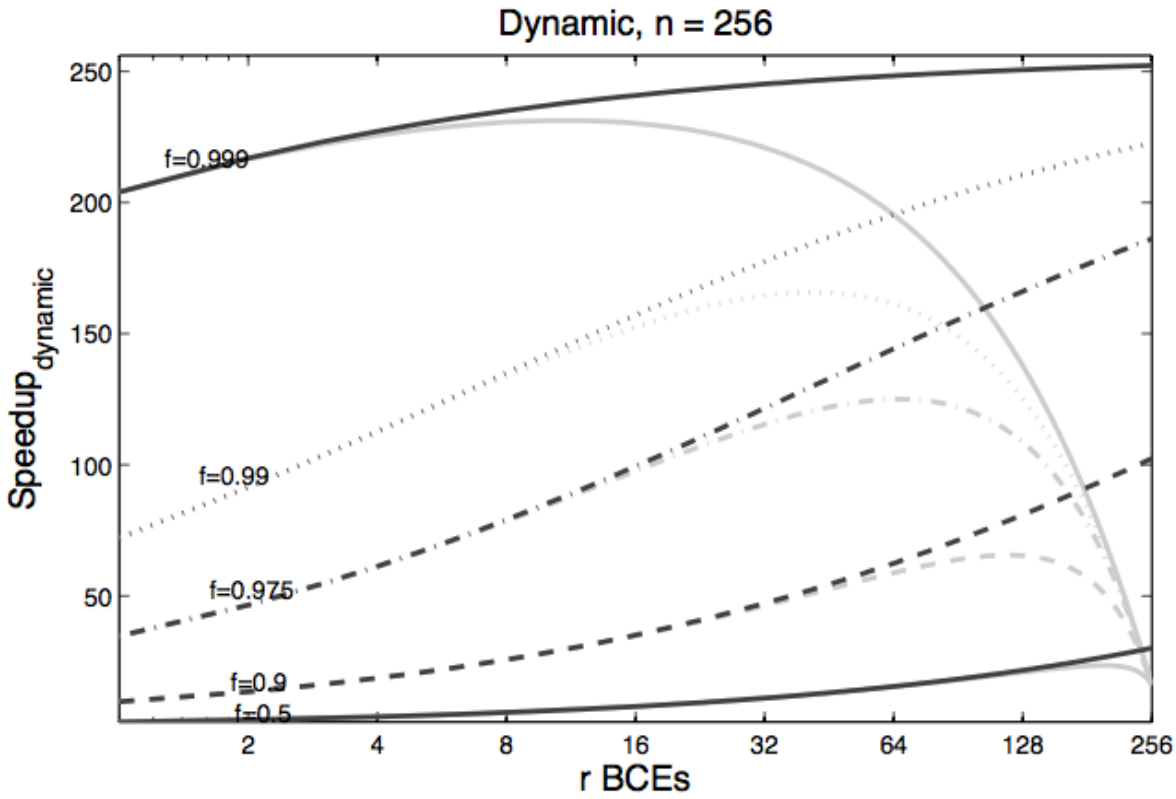


Figure: Speedup for dynamic chip design

$$f = 0.975 \ \textit{Best Speedup}_{asymmetric} = 125.0$$

$$f = 0.975 \ \textit{Corresponding Speedup}_{dynamic} = 145.0$$

Implications

- Increasing core performance to be globally efficient.

- Symmetric multicore designs do not give effective speedups
- Asymmetric multicore designs offer greater potential speedups
- Dynamic designs have the potential to achieve the best speedups

Summary

- Three types of chip designs: symmetric, asymmetric, dynamic
- Simulation results for the chips designs imply that dynamic designs work best.

Thank you !